REMARKS

Claim 2, as objected to, has been incorporated into claim 1. Claims 12 and 15 have been amended to include their base and intervening claims as required by the Examiner.

The Applicants believe that the subject application, as amended, is in condition for allowance. Such action is earnestly solicited by the Applicants.

In the event that the Examiner deems the present application non-allowable, it is requested that the Examiner telephone the Applicant's attorney or agent at the number indicated below so that the prosecution of the present case may be advanced by the clarification of any continuing rejection.

Accordingly, this application is believed to be in proper form for allowance and an early notice of allowance is respectfully requested.

Please charge any fees associated herewith, including extension of time fees, to 13-4771.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.
Law Department

Customer Number: 23330

By: _____
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MARKED UP VERSION OF CLAIMS AMENDED IN REWRITTEN FORM

CLAIMS

1.(AMENDED) A circuit for interleaving a data stream, comprising:

a buffer storage circuit having an input coupled for receiving and storing the data stream;

a first memory circuit having an input coupled to an output of the buffer storage circuit for receiving a first section of the data stream;

a second memory circuit having an input coupled to the output of the buffer storage circuit for receiving a second section of the data stream wherein the first and second sections of the data stream are representative of different channels of an audio signal; and

a multiplexer circuit having first and second inputs respectively coupled to the outputs of the first and second memory circuits for selecting between the first and second sections in response to a selection signal to provide an interleaved output signal at an output.

12.(AMENDED) [The method of claim 11,] A method of interleaving a data stream, comprising the steps of:

storing the data stream including storing data of the first section of the data stream and data of the second section of the data stream in a third memory location;

copying a first section of the data stream to a first memory location;

copying a second section of the data stream to a second memory location;

selecting between the first and second memory locations to produce an interleaved output signal and selecting between data stored in the first memory location and data stored in the second memory location, wherein the step of selecting further includes the step of selecting first data from the first memory location while transferring second data from the third memory location to the first memory location.

15.(AMENDED) [The method of claim 14, wherein the step of selecting the first data further includes the steps of:] A method of interleaving a data stream, comprising the steps of:

storing the data stream including storing data of the first section of the data stream and data of the second section of the data stream in a third memory location;

copying a first section of the data stream to a first memory location;

copying a second section of the data stream to a second memory location;

selecting between the first and second memory locations to produce an interleaved output signal and selecting between data stored in the first memory location and data stored in the second memory location, wherein the step of selecting includes:

transferring data from the third memory location to the first memory location in response to a first control signal; and

incrementing a first pointer representative of an amount of data stored in the first memory location;

decrementing the first pointer as data stored in the first memory location is selected; and

generating the first control signal after the first pointer decrements to a first predetermined value.

19.(AMENDED) An integrated circuit, comprising:

a buffer storage circuit having an input coupled for receiving and storing a multimedia data stream;

a first memory circuit having an input coupled to an output of the buffer storage circuit for receiving a first section of the multimedia data stream;

a second memory circuit having an input coupled to the output of the buffer storage circuit for receiving a second section of the multimedia data stream wherein the first and second sections of the data stream are representative of different channels of an audio signal; and

a multiplexer circuit having first and second inputs respectively coupled to the outputs of the first and second memory circuits for selecting between the first and second sections in response to a selection signal to provide an interleaved output signal at an output.